TABLE 3

| Function | Exclusive cycle count C674x per biquad | Exclusive cycle count C66x per biquad | C66x/C674x Improvement | C674x bytes | C66x bytes | Comments C674xx | Comments C66x |
|---|---|---|---|---|---|---|---|
| Cascade Biquad 1 Channel 2 stage | 4.5 | 4 | 1.11x | 268 | 416 | Loop Carried Dependency Bound 8, Resource bound is 4 | Loop Carried Dependency Bound 16, Resource bound is 7 Loop Unroll 2x |
| Cascade Biquad 2 channel 4-stage, same coefficient | 2.125 | 1.375 | 1.35x | 1128 | 904 | Loop Carried Dependency Bound 8, Resource bound is 16 | Loop Carried Dependency Bound 10, Resource bound is 8 |
| Cascade Biquad 2 channel 3-stage, same coefficient | 2 | 1.33 | 1.34x | 536 | 656 | Loop Carried Dependency Bound 10, Resource bound is 12 | Loop Carried Dependency Bound 8, Resource bound is 7 |

TABLE 4

| Cascaded Biquad | Exclusive cycle count C674x per biquad | Exclusive cycle count C66x per biquad | C66x/C674x Improvement | Comments C674xx | Comments C66x |
|---|---|---|---|---|---|
| 1 Channel 2 stage Single Precision | 4.5 | 4 | 1.11x | Loop Carried Dependency Bound 8, Resource bound is 4 | Loop Carried Dependency Bound 16, Resource bound is 7 Loop Unroll 2x |
| 1 Channel 2 stage, same coefficient, Mixed/Double Precision | 9.75 | 4 | 2.4x | Loop Carried Dependency Bound 37, Resource Bound is 32 Loop Unroll 2x | Loop Carried Dependency Bound 10, Resource Bound is 10 |
| 1 Channel 3 stage, same coefficient, Mixed/Double Precision | 15.33 | 3.33 | 4.6x | Loop Carried Dependency Bound 20, Resource Bound is 24 | Loop Carried Dependency Bound 8, Resource Bound is 9 |
| 2 Channel 2 stage, same coefficient, Mixed/Double Precision | 15.25 | 3.5 | 4.36x | Loop Carried Dependency Bound 17, Resource Bound is 32 | Loop Carried Dependency Bound 7, Resource Bound is 14 |

What is claimed is:

**1**. A method of performing infinite impulse response filtering, the method comprising the steps of:

computing the filter output by setting

out=in+d0

t1=(b1+a1)*in+d0

t0=a2*d0

d0=a1*d0

d1=(b2+a2)*in+t0

where a1, a2, b1, b2 are coefficients and d0, d1, t0, t1 are intermediate results.

**2**. The method of claim **1**, wherein:

the output is computed using a digital signal processor.

**3**. The method of claim **1**, wherein:

the digital signal processor is a very long instruction word type of digital signal processor.

**4**. An apparatus for performing infinite impulse response filtering, the apparatus comprising:

a digital signal processor operable to compute the filter output by performing the following steps:

out=in+d0

t1=(b1+a1)*in+d0

t0=a2*d0

d0=a1*d0

d1=(b2+a2)*in+t0

where a1, a2, b1, b2 are coefficients and d0, d1, t0, t1 are intermediate results.

**5**. The apparatus of claim **4**, wherein:

the digital signal processor is a very long instruction word type of digital signal processor.

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